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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,856	02/19/2004	Yasushi Inagaki	041226-0307277	2465

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EXAMINER	
DINH, TUAN T	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 08/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/780,856	INAGAKI ET AL.	
	Examiner	Art Unit	
	Tuan T. Dinh	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,9,10,15,75 and 79-90* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,9,10,15,75 and 79-90* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05/25/06 has been entered.

Claim Objections

2. Claim 88 is objected to because of the following informalities:

Claim 88, lines 1-2, please delete "the capacitor is a ceramic capacitor" because the phrase has been defined in claim 86, line 6 for proper reading.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 15 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 15, lines 7-9, it is unclear. The phrase of "a CTE of the insulating bonding agent is ***lower than that of*** said first resin substrate" is not understood. Does applicant mean of "the CTE of the insulating agent is lower than a CTE of the first resin substrate? Please, clarify.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 5, 9, 15, 75, 79, 83-85 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamashita (U.S. Patent 5,875,100), as in the record.

As to claims 1, 5, Yamashita discloses a printed circuit board as shown in figures 1A-1G comprising:

a core substrate comprising a first resin substrate (30), a second resin substrate (20) having an opening (21) and a third resin substrate (element 30 located at a bottom of the substrate 20) in a multilayer manner while interposing bonding plates;

insulating layers and conductive circuit layers (these elements formed in the substrates 30 and laminated on top and bottom to the element 20) alternately laminated on the core substrate;

a semiconductor chip (10, column 2, line 67), which is a capacitor (column 4, line 67 through column 5, line 2) formed in the opening (21) of the second resin substrate (20);

first and second conductive pads (11) formed on the first resin substrate and connected to electrodes (12) of the chip, see figure 2;

first and second via holes (40, the electrodes 12 exposed into via holes of the first substrate 30, see figures 1E-1G) in formed in the first resin substrate, the first and second via hole directly connected to the first conductive pad and a conductive circuit on the core substrate, the conductive circuit formed on the second resin substrate (20), claim 5.

As to claim 15, Yamashita discloses a printed circuit board as shown in figure 1G constituted by alternately laminating insulating layers and conductive circuits, see figure 1G on a core substrate containing a ceramic capacitor (10, an insulating material of the capacitor 10 inherently made by ceramic), wherein the core substrate containing said capacitor (10) comprises a first resin substrate (top layer 30), a second resin substrate (20) having an opening (21) and a third resin substrate (a bottom layer 30) in a multilayer manner while interposing bonding plates, said first resin substrate (30) and said ceramic capacitor (10) are coupled to each other by an insulating bonding agent and having a coefficient of thermal expansion (CTE) and connected to an electrode (12) of the capacitor, and a via hole (40), through which the conductive pad is connected to the conductive circuit on the core substrate, is formed in the first resin substrate.

As to claims 75, 83, Yamashita discloses a printed circuit board as shown in figures 1-2 comprising:

a core substrate comprising a first resin substrate (top layer 30),

a second resin substrate (layer 20) having an opening (21) and a third resin substrate (bottom layer 30) in a multilayer manner while interposing bonding plates;

insulating layers and conductive circuit layers alternately laminated on the core substrate,

a plurality of bumps (column 9, lines 9-26) formed on an outer layer of the insulating layers and constituting a bump area; and

a capacitor (10) formed in the opening (21) of the second resin substrate and located immediately below the bump area; wherein at least one of the bumps is electrically connected to an electrode of the capacitor through a via hole (40) formed in the core substrate, the via hole formed immediately below the bump area, and an IC (60) electrical connected to said bump.

As to claims 9, 79, Yamashita further comprising a metal film (51) formed on the electrode of said capacitor (10).

As to claims 84-85, Yamashita further comprising a plurality of bumps (column 6, lines 9-26) formed on an outer layer of the insulating layers and constituting a bump area, wherein at least one of the bumps is electrically connected to the electrode of the capacitor through a via hole formed immediately below the bump area, and an IC chip (60) is to be mounted on the bump area.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2-3, 81-82 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita in view of Sakaguchi et al. (5,873,624).

Regarding claims 2-3, and 81-82, Yamashita discloses all of the limitations of the claimed invention, except for each of said bonding plates having said first, second and third resin substrates having a core made of glass cloth and a resin impregnated with a thermosetting resin.

Sakaguchi teaches a printed wiring board as shown in figures 1-5 comprising an insulating material having a core made of glass cloth and a resin impregnated with a thermosetting resin.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have an insulating material having a core made of glass cloth and a resin impregnated with a thermosetting resin as taught by Sakaguchi employed in one of the substrates of the PCB of Yamashita in order to provide a CTE mismatch and flexure on the PCB.

9. Claims 2-4, 10, 80-82, and 86-90 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita in view of Ehman et al. (U.S. Patent 6,021,050).

As to claims 2-4, 81-82, and 86-90, Yamashita discloses all of the limitations of the claimed invention, except for each of said bonding plates having said first, second and third resin substrates having a core made of glass cloth and a resin impregnated with a thermosetting resin, and a plurality of openings and capacitors formed in the openings.

Ehman et al. teaches a printed wiring board as shown in figures 1-3 comprising layers (12, 14, and 16) each made of glass cloth and a resin impregnated with a thermosetting resin.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have layers made of glass cloth and a resin impregnated with a thermosetting resin as taught by Ehman employed in one of the substrates of the PCB of Yamashita in order to provide a CTE mismatch and flexure on the PCB.

As to claims 10, 80, Yamashita discloses all of the limitation of the claimed invention, except for the metal film formed on the electrode of said capacitor is a plated film mainly consisting of copper.

Ehman teaches copper conductor circuit paths 30, 32 formed on a surface of the capacitor 26.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have copper path formed on the capacitor as taught by Ehman employed in one of the substrates of the PCB of Yamashita in order to provide good electrical conductivity.

Response to Arguments

10. Applicant's arguments with respect to claims 1-5, 9-10, 15, 75, and 79-90 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tuan Dinh
July 31, 2006.